MODELING AND PSPICE SIMULATION OF RADIATION STRESS INFLUENCE ON THRESHOLD VOLTAGE SHIFTS IN P-CHANNEL POWER VDMOS TRANSISTORS*

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Abstract. In this paper the results of modeling and simulation of radiation stress effects in p-channel power VDMOSFET transistor have been presented. Based on measured results, the threshold voltage shifts as a function of absorbed dose and gate voltage during radiation stress have been modeled and implemented in the PSPICE model of the IRF9520 transistor. The transfer characteristics of the transistor are simulated and compared to the experimental ones. Difference is in the range 0.16% to 23.35% which represents a good agreement.

Key words**:** *radiation stress effect, modeling, PSPICE simulation, VDMOS transistor*

DOI: 10.21175/RadJ.2016.01.05

1. INTRODUCTION

Different analytical models are used for characterization and PSPICE simulations of electronic devices. The extraction of the model parameters from experimental results is the crucial step in that procedure. By adding specific elements to basic circuit model, such as parametrically controlled voltage sources [1], external stress influence to operation of the device can be modeled.

The power vertical double-diffused MOSFETs (VDMOSFET) are suitable for use in electronics, which may operate in radiation environments, due to their high switching speed, simplified input drive requirements, low noise, etc. Power VDMOSFETs are attractive devices for high-frequency switching power supplies in communication satellites because of their high radiation tolerance during the years of communication satellite missions. This is the reason why many scientists nowadays express interest to the investigation of radiation stress effects in VDMOS transistors [2-4]. It should be noted that there is interest in analytical modeling of device characteristics under radiation, with the aim to predict the device behavior in real radiation environment. [5]

In this paper the procedure for PSPICE modeling of radiation stress effects in p-channel power VDMOS transistor IRF9520 is presented. In these devices, radiation stress effects occur when they are exposed to radiation sources. The proposed model can be used for simulation cases when devices are exposed to relatively small doses (0 – 75 Gy), for gate voltages during stress in the range from -10 V to +10 V. Influences of degradation effects on the threshold voltage values are considered here.

2. RADIATION STRESS EFFECTS ON THRESHOLD VOLTAGE SHIFTS

2.1. Theoretical overview

When VDMOSFET is exposed to ionizing radiation, electrons and holes are created in the device as a result of ionization. Most of the free electrons eventually recombine and they do not contribute to the threshold voltage shift. The charge carriers providing the threshold voltage shift are the holes trapped in the gate oxide [6]. A certain number of induced holes also recombine immediately after generation. However, radiation-induced holes which do not recombine will be drifted by the influence of the electric field, and trapped on oxide defects leading to the creation of positive charge in the gate oxide. The hole traps exist as an intrinsic part of the gate oxide because of structural defects. Also, holes get trapped at the Si/SiO_2 interface states precursors created positive interface charge. Both the positive charge generated in the SiO_2 layer and the interface states increase the absolute value of the threshold voltage in p-channel VDMOSFETs.

The traps induced in the gate oxide are referred to as oxide or fixed traps, while the traps created near and at the oxide/substrate (SiO_2/Si) interface are known as interface or switching traps. The interface traps created in the oxide, near the SiO_2/Si interface, are called the slow switching traps and the interface traps created at this interface are called the fast switching traps. The fixed traps represent traps in the gate oxide that do not capture the carriers from the channel, while the switching traps represent the traps that do capture the carriers from the channel.

[*] The paper was presented at the Third International Conference on Radiation and Applications in Various Fields of Research (RAD 2015), Budva, Montenegro, 2015.

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2.2. Experimental results

Experimental I-V characteristics in the saturation regime of IRF9520 transistor are used for PSPICE model setup. Obtained experimental transfer characteristics are set as reference for fitting procedures and comparison of simulation results. Radiation of devices was performed in Vinča Institute for Nuclear Sciences using Co^{60} gamma radiation source at gate voltages of V_{GATE}={+10 V, -10 V, 0 V}. The dose rate was 8.33 mGy/s. The transistors were read-out before stressing, after 20, 40, 70, 110 and 150 minutes, corresponding to total absorbed doses 10, 20, 35, 55 and 75 Gy, respectively. For example, Fig. 1 illustrates typical experimental transfer characteristics of transistor during gamma radiation stressing at V_{GATE}=+10 V, obtained at some specific dose levels. As can be seen, the characteristics are shifted along the V_{GS} axis which indicate that there is a change in the threshold voltage with changing of radiation dose. The system used for measurement of the transfer characteristics during gamma radiation, is presented in details in [7].

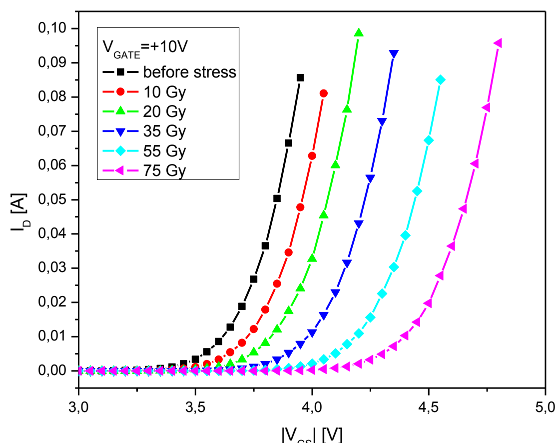

Figure 1. Experimental transfer I-V characteristics of p-channel power VDMOS transistor IRF9520 during gamma radiation stressing at V_{GS}=+10 V

2.3. Modeling of the threshold voltage shifts

VDMOS transistor IRF9520 is modeled in PSPICE as a subcircuit whose main part is PMOS transistor (level 3) [8]. During the model setup, threshold voltage is defined as the main electrical parameter of MOS transistor. The threshold voltage of commercial p-channel IRF9520 transistors is in the range from -2 V to -4 V [9], making difficulties to generate an universal PSPICE model of this transistor. First, the threshold voltage V_T is estimated from the transfer characteristics in saturation, as the intersection of extrapolated linear region of $\sqrt{I_D}$ with V_{GS} axis [10]. Based on the experimental results, for the threshold voltage values before radiation stressing (V_{TO}) the values of -3.5178 V (for samples radiated when V_{GATE}=+10 V), -3.5994 V (V_{GATE}=-10 V) and -3.5873 V (V_{GATE}=0 V) were used.

The dependence between the threshold voltage shift (ΔV_T), and the absorbed dose (D) can be approximated as:

$$\Delta V_T = a \cdot D^n \qquad (1)$$

where $\Delta V_T = V_T - V_{To}$, V_T is the threshold voltage after radiation, V_{To} before radiation, a is a constant, and n is the degree of linearity. The parameter n depends on oxide thickness, electric field and total absorbed dose; and n can be in the range of 0.6 to 0.98 [11]. In our case, n=1 because proposed model is for small dose of radiation. Several studies have shown that expression (1) does not represent realistically the response of VDMOSFET at very high doses because ΔV_T saturates in practice [11, 12]. In terms of physics, the induced positive charge increases with the increase of absorbed dose, and therefore the threshold voltage shift is proportional to the absorbed dose as defined by the (1).

During radiation, VDMOSFET can be in zero-bias or biased mode. In zero-bias mode all terminals (gate, drain, source/bulk) are grounded. It should be noted that VDMOSFETs are three terminal devices with the bulk region internally connected to source. In biased mode, gate is biased with positive or negative voltage (usually ±5V or ±10V) while other terminals are grounded. A number of studies have confirmed that the sensitivity increases linearly with the applied gate bias voltage, whereby the sensitivity is higher for positive bias than for negative bias [12]. Namely, positive gate bias applied to the gate of PMOS transistors causes majority carrier accumulation in n-bulk under gate oxide, while negative gate bias causes strong inversion. Surface potential in accumulation is significantly lower than in strong inversion and electric field in the oxide is stronger in case of positive gate bias. Moreover, radiation created positive oxide charge shifts flat band voltage to negative direction, which additionally enhances electric field in the oxide in the case of positive gate bias, and therefore radiation effects are more pronounced. Generally, for both positive and negative gate bias, the sensitivity increases with the increase of the absolute value of voltage bias applied on the gate terminal. However, the practical value of the applied biasing voltage is limited by the power supply voltage used in a specific application. The dependence between the parameter a from (1) and gate voltage V_{GATE} during radiation can be expressed in the form:

$$a = A + BV_{GATE} + CV_{GATE}^2 \qquad (2)$$

where A, B and C are fitting parameters obtained from experimental results. The expression (2) is applicable only for samples with the same gate oxide thickness, because for different oxide thicknesses the sensitivity to radiation will differ.

2.4. PSPICE simulation of the threshold voltage shifts

The electrical schematic implemented in PSPICE is shown in Fig. 2. The effect of radiation stressing is included in PSPICE by adding two auxiliary voltage generators (*DOSE* and V_{GATE}) in the model of IRF9520 transistor. The value of generator *DOSE* is amount of absorbed dose, and value of generator V_{GATE} is gate bias voltage during radiation. Transistor is configured to operate in the saturation region for simulation of the

$I_D=f(V_{GS})$ characteristics. Value of the voltage V_{DD} in simulation was in the range of 0 to -5 V.

The ***.PARAM*** function allows easy entering of necessary model parameters, such as DOSE, VGATE, A, B and C parameters. By using PSPICE command ***.FUNC***, whose parameters are dose and gate voltage during stress, the threshold voltage shift is determined according to expressions (1) and (2). Obtained value of the threshold voltage shift is used as input parameter in PSPICE netlist for generation of the transfer characteristics. Since irradiation seriously affects channel carrier mobility, it was necessary to include this effect. The slope of the transfer characteristic is determined by transconductance parameter (*KP*) value, and by tuning of this parameter the simulated and experimental characteristics are matched.

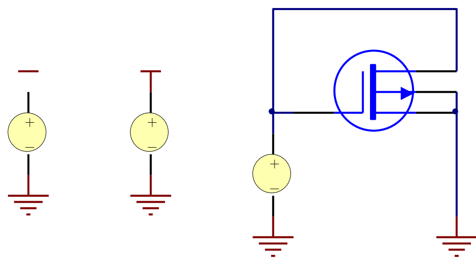

Figure 2. Electrical schematics of VDMOS transistor IRF9520 with auxiliary voltage generators DOSE and VGATE for simulation of the transfer characteristics.

3. RESULTS AND DISCUSSION

Extensive simulations have been performed in order to test the proposed model characteristics. The model has passed all performed tests and can be used to analyze various complex circuits with VDMOS transistor IRF9520 to simulate influence of radiation stress. The simulation results are compared with the measured ones for this transistor.

Based on the measured results, variation of threshold voltage shift with absorbed dose for various gate bias levels during radiation was obtained and it is shown in Fig. 3. As can be seen, dependence is linear so that by applying linear fitting, slope coefficients of lines are determined. The values of coefficients are: a=0.01031 V/Gy (for transistors biased with +10 V at gate during the radiation), a=0.00894 V/Gy (V_{GATE}=-10 V) and a=0.00279 V/Gy (V_{GATE}=0 V). In all cases, intercept value in equation of line is equal to 0.

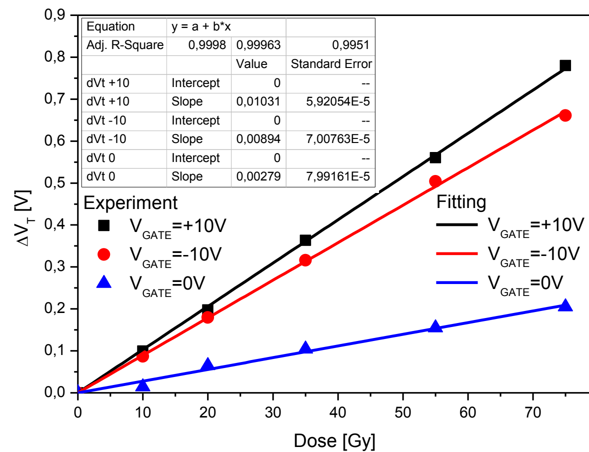

Figure 3. Variation of threshold voltage shift with absorbed dose for various gate bias levels.

Fig. 4 shows experimentally determined parameter a as a function of gate bias voltage during radiation stress (V_{GATE}). Dependence of parameter a on V_{GATE} is approximated with the so called parabola function given by the expression (2). Obtained fitting parameters are: A=0.00279 V/Gy, B=6.9185·10^{-5} V^{-1} and C=6.835·10^{-5} V^{-2}. By using these parameters (A, B and C) and assigning an arbitrary gate voltage during radiation (V_{GATE}), for a given dose of radiation ($DOSE$), threshold voltage shift will be completely determined. Values of threshold voltage before and during radiation obtained by experiment and simulation are given in Table 1. It is obvious that there is a small disagreement between threshold voltages, ranging from 0.03% to 0.38%. The calculated relative error of the simulated threshold voltages shift compared to experimental values vs. dose is in the range of 0.47 % to 16.13%.

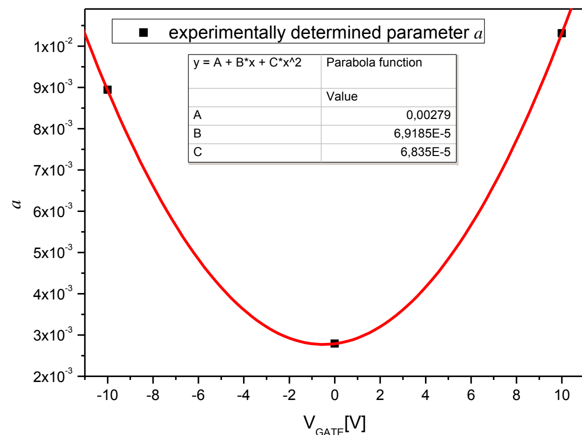

Figure 4. Parameter a as a function of V_{GATE}.

Table 1. Threshold voltage before and during radiation (experiment and simulation)

VGATE [V]	0		+10		-10	
DOSE [Gy]	Meas.	Sim.	Meas.	Sim.	Meas.	Sim.
0	3.587	3.587	3.518	3.518	3.599	3.599
10	3.602	3.615	3.617	3.621	3.686	3.689
20	3.652	3.643	3.715	3.724	3.779	3.778
35	3.692	3.685	3.881	3.879	3.915	3.912
55	3.742	3.741	4.078	4.085	4.103	4.091
75	3.792	3.797	4.297	4.291	4.26	4.269

For example, measured and simulated transfer characteristics of transistor IRF9520 for three different gate bias voltages during radiation stress (0 V, +10 V and -10 V) and doses (20 Gy, 35 Gy and 55 Gy), respectively, are shown in Fig. 5. Good matching of these characteristics is achieved by adjusting transconductance parameter *KP* directly in PSPICE model. Values of *KP* are in range from $1.78 \cdot 10^{-5}$ to $2.34 \cdot 10^{-5}$. Similar results are obtained for other combinations of the gate voltage and dose.

Fig. 6 presents relative errors of the simulated drain current comparing to the experimental values as a function of the gate-source voltage (Fig. 5). For all investigated devices, the relative error is in the range (0.16 – 23.35) % for gate-source voltages above the threshold. It is evident that, there is a good agreement between simulated and experimental characteristics in the region above the threshold voltage, but for the subthreshold region this is not the case. The proposed model should be extended for simulation of radiation stress effects in the subthreshold region. However, if we consider using of here extended PSPICE model of power VDMOSFET in simulation of electronic systems where these devices could be used, disagreement in the subthreshold region is of much lower interest, excluding importance of device leakage current.

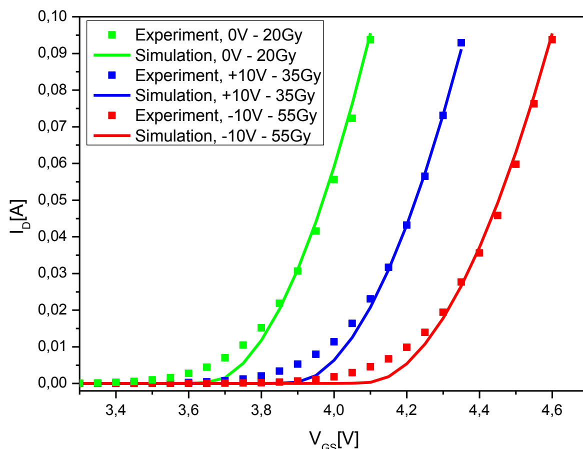

Figure 5. Experimental and simulated transfer characteristics of transistor IRF9520 for different doses and gate voltages during radiation.

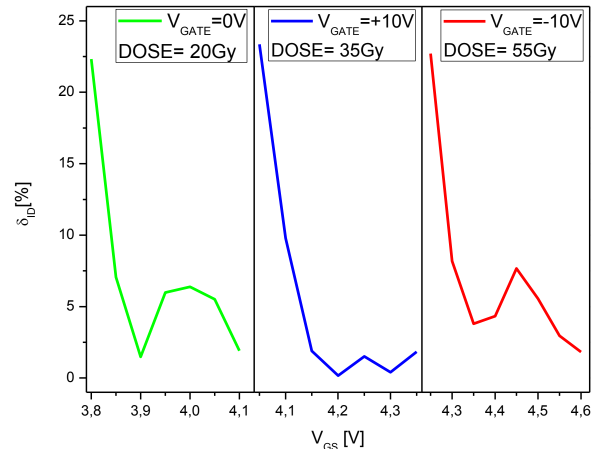

Figure 6. Relative error of the simulated drain current compared to experimental values vs. gate voltage V_{GS}.

4. CONCLUSION

Results of the modeling and PSPICE simulation of radiation stress effects in p-channel power VDMOSFET transistors IRF9520 are presented. Based on the experimental data, threshold voltage shifts due to radiation stressing (parameters *a* and *DOSE*) are implemented into PSPICE model of the transistor. Appropriate analytical approximation of parameter *a* in function of gate voltage during radiation is proposed. Threshold voltage shift is modeled by two auxiliary parametrically controlled voltage generators. By iterative fitting of the simulated characteristics to the experimental ones, the value of transconductance parameter *KP* is determined. The proposed model gives transfer characteristics which are close to the measured ones. These characteristics are within (0.16 % to 23.35 %) limits in respect to the experiment in the region above the threshold. The main drawback of this model is inability to model the subtreshold characteristics. Developing of model for subthreshold region and establishing the overall model of p-channel VDMOSFET power transistors with radiation stress effects are our future tasks.

Acknowledgement: *The authors gratefully acknowledge the financial support of Serbian Ministry of Education, Science and Technological Development. This research is a part of the projects OI 171026 and TR 32026.*

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